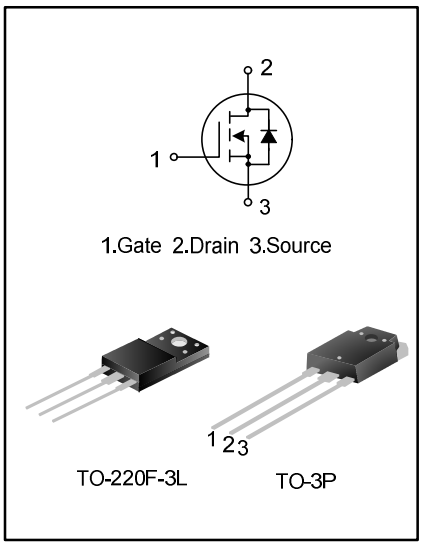
20A, 500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF20N50F/PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

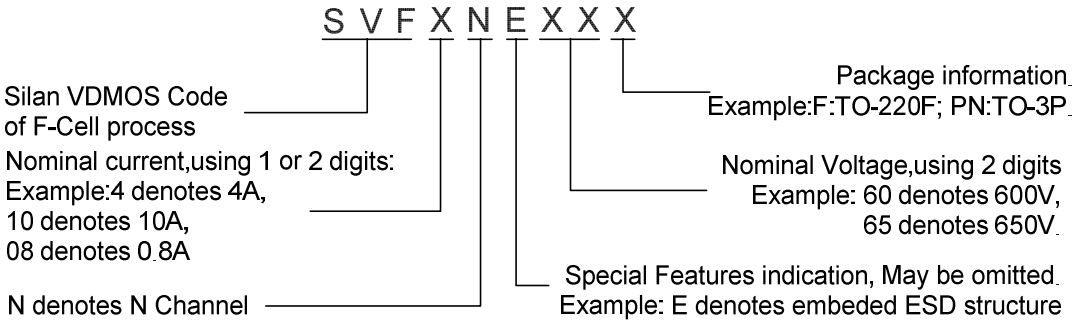
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 20A,500V,$R_{DS(on)(typ.)}$=0.20Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF20N50F	TO-220F-3L	SVF20N50F	Pb free	Tube
SVF20N50PN	TO-3P	20N50	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVF20N50F	SVF20N50PN	
Drain-Source Voltage		V_{DS}	500		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	20.0		A
	T_C=100°C		12.6		
Drain Current Pulsed		I_{DM}	80.0		A
Power Dissipation(T_C=25°C)		P_D	72	252	W
-Derate above 25°C			0.58	2.02	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	1596		mJ
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF20N50F	SVF20N50PN	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.74	0.50	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	50	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	500	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10.0A	--	0.20	0.27	Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	2687.7	--	pF
Output Capacitance	C_{oss}		--	355.0	--	
Reverse Transfer Capacitance	C_{rss}		--	10.3	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=250V, I_D=20.0A, R_G=10Ω, (Note2,3)	--	27.2	--	ns
Turn-on Rise Time	t_r		--	47.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	78.7	--	
Turn-off Fall Time	t_f		--	41.1	--	
Total Gate Charge	Q_g	V_{DS}=400V, I_D=20.0A, V_{GS}=10V, (Note 2,3)	--	49.50	--	nC
Gate-Source Charge	Q_{gs}		--	14.28	--	
Gate-Drain Charge	Q_{gd}		--	16.95	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	20.0	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	80.0	
Diode Forward Voltage	V_{SD}	I_S=20.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=20.0A,V_{GS}=0V,	--	570.3	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μs (Note 2)	--	7.35	--	μC

Notes:

1. L=30mH, I_{AS}=9.9A, V_{DD}=50V, R_G=25Ω, starting TB_{JB}=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

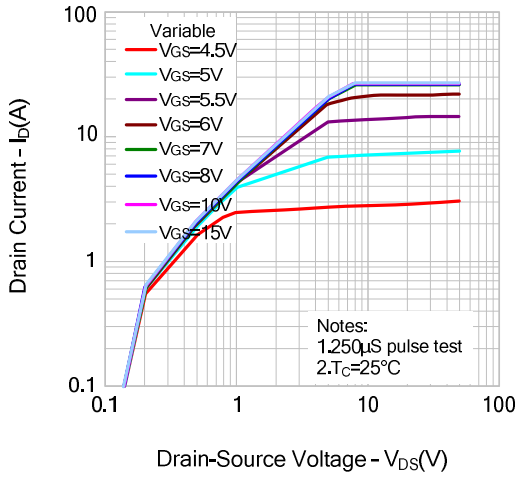


Figure 2. Transfer Characteristics

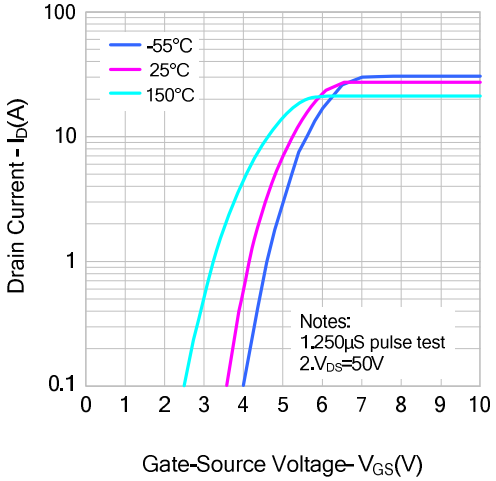


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

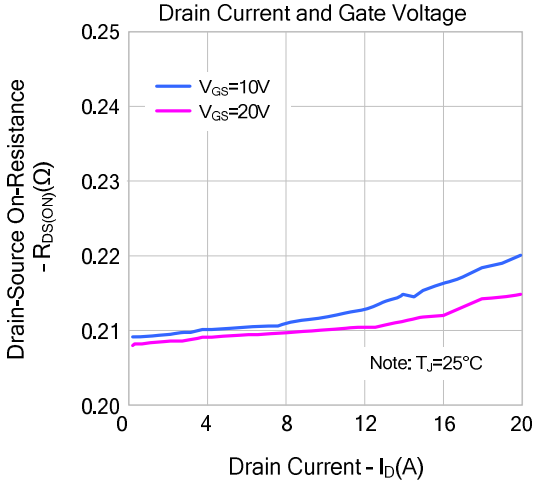


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

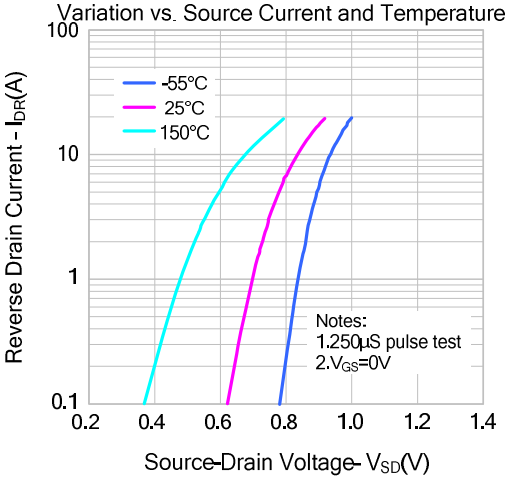


Figure 5. Capacitance Characteristics

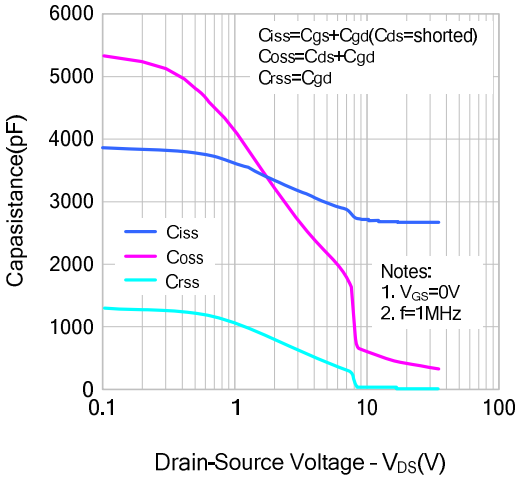
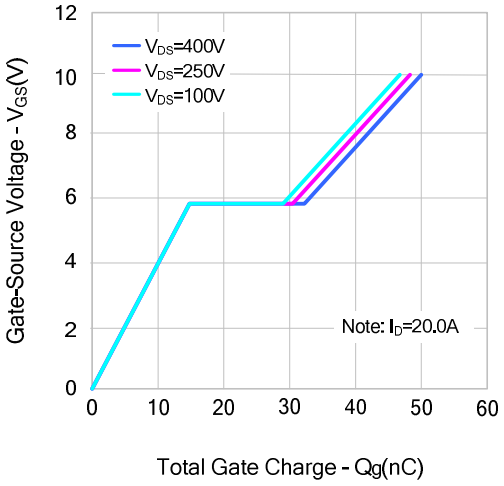


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

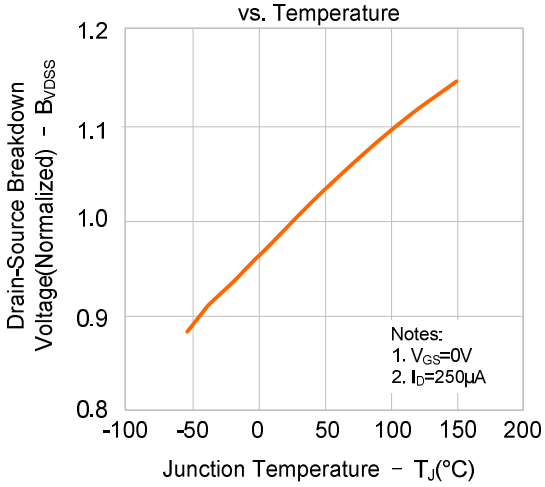


Figure 8. On-resistance Variation vs. Temperature

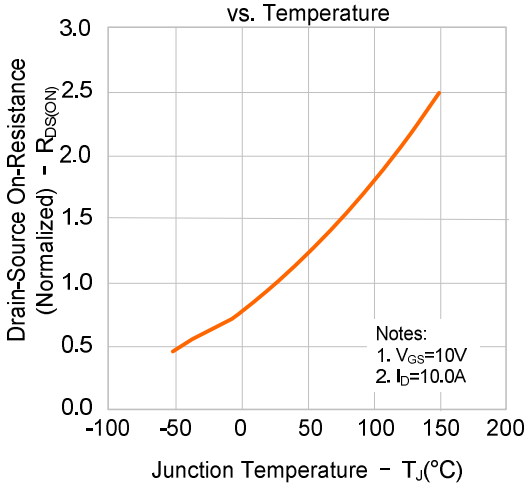


Figure 9-1. Max. Safe Operating Area (SVF20N50F)

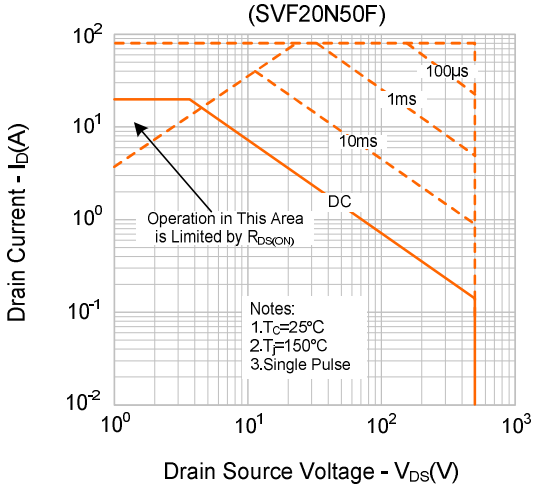


Figure 9-2. Max. Safe Operating Area (SVF20N50PN)

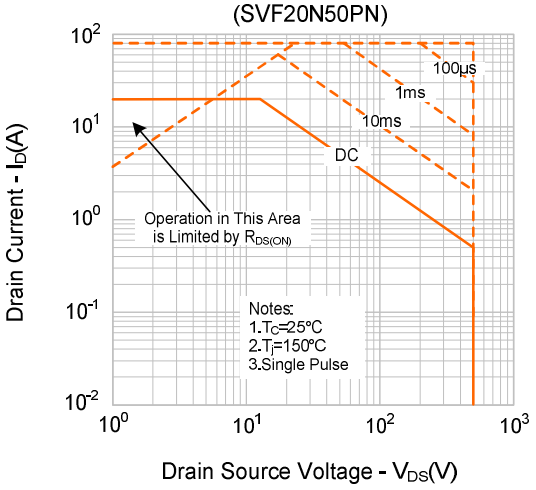
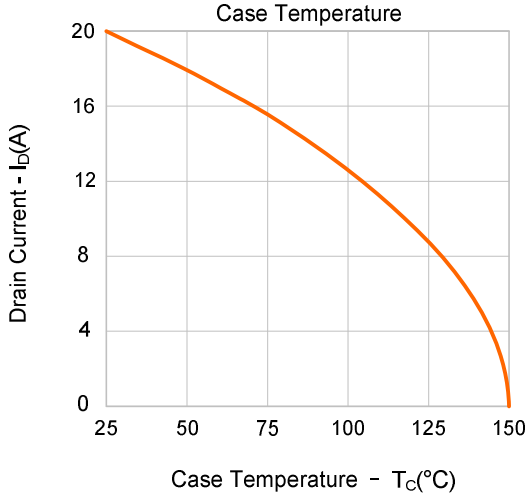
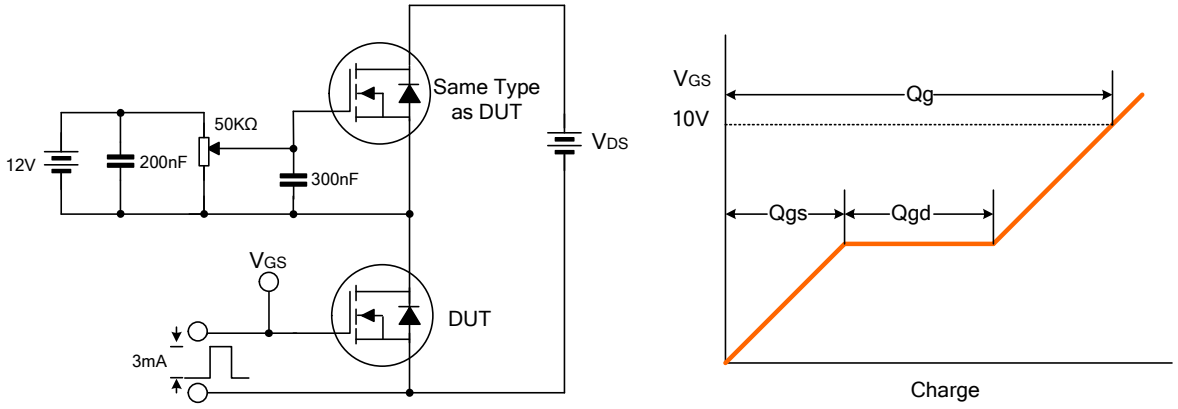


Figure 10. Maximum Drain Current vs. Case Temperature

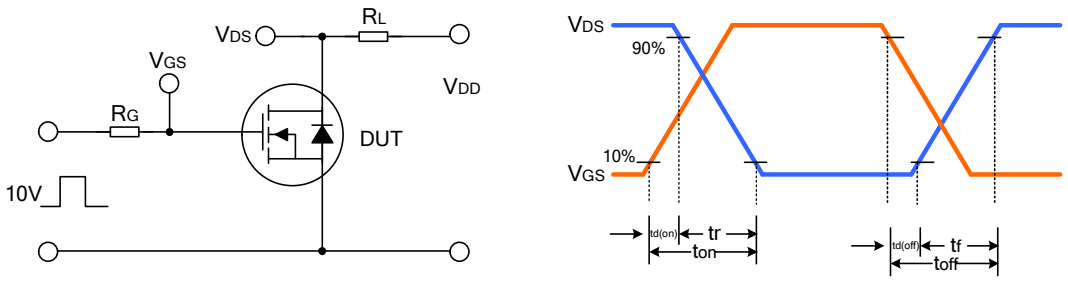


TYPICAL TEST CIRCUIT

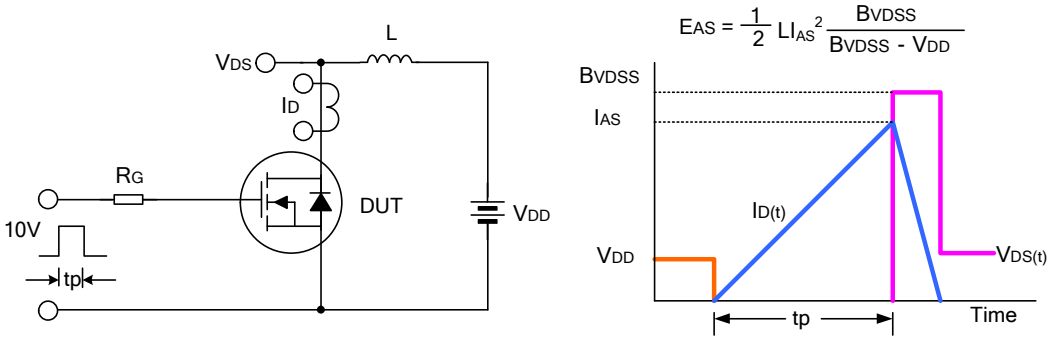
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



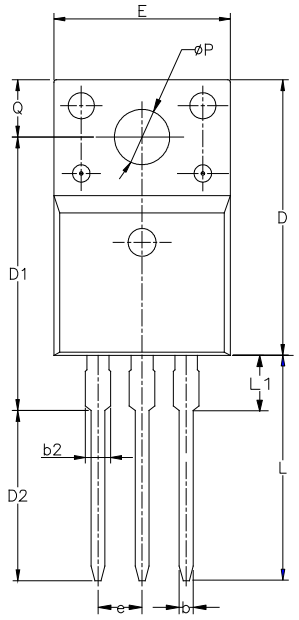
Unclamped Inductive Switching Test Circuit & Waveform

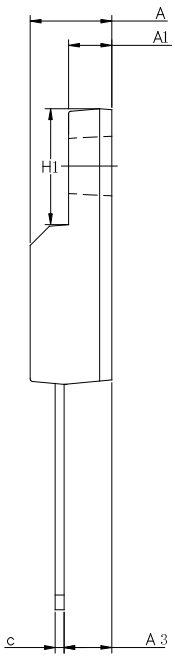


PACKAGE OUTLINE

TO-220F-3L

UNIT: mm

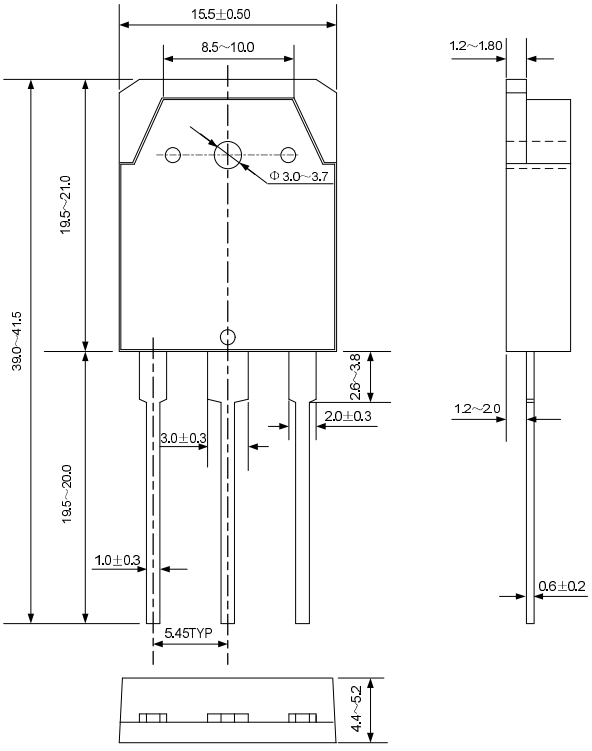




SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-3P

UNIT: mm



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Revision History:

1. Modify the package information of TO-220F-3L

Rev.:	1.4	Author:	Yin Zi

Revision History:

1. Modify the thermal characteristics

Rev.:	1.3	Author:	Yin Zi

Revision History:

1. Modify the ordering information

Rev.:	1.2	Author:	Zhang Kefeng

Revision History:

1. Change the schematic diagram of MOS

Rev.:	1.1	Author:	Zhang Kefeng

Revision History:

1. Add the package of TO-3PN
2. Modify “ELECTRICAL CHARACTERISTICS” and “TYPICAL CHARACTERISTICS”

Rev.:	1.0	Author:	Zhang Kefeng

Revision History:

1. Initial release