NTMFS5H409NL

Power MOSFET
40 V, 1.1 mΩ, 270 A, Single N−Channel

Features
- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	1.1 mΩ @ 10 V	270 A
	1.6 mΩ @ 4.5 V	

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{θJC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	270	A
		T_C = 100°C		170	
Power Dissipation $R_{θJC}$ (Note 1)		T_C = 25°C	P_D	140	W
		T_C = 100°C		56	
Continuous Drain Current $R_{θJA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	41	A
		T_A = 100°C		26	
Power Dissipation $R_{θJA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.2	W
		T_A = 100°C		1.3	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	160	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 45 A)			E_{AS}	304	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

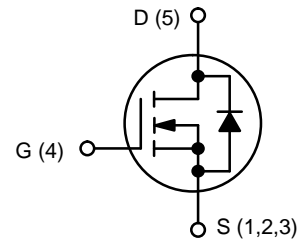| Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{θJC}$	0.9	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{θJA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
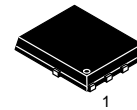3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

D (5)

G (4)

S (1,2,3)

N−CHANNEL MOSFET

**DFN5
(SO−8FL)
CASE 488AA
STYLE 1**

MARKING DIAGRAM

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      D
S ┌──────┐ D
S │5H409L│ D
S │AYWZZ │
G └──────┘ D
      D
```
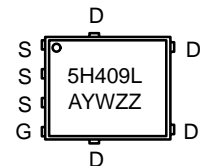
5H409L = Specific Device Code
A   = Assembly Location
Y   = Year
W   = Work Week
ZZ   = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				19.1		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			1.0	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−4.8		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		0.85	1.1	mΩ
		V_{GS} = 4.5 V	I_D = 50 A		1.2	1.6	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 50 A			300		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V			5700		pF
Output Capacitance	C_{OSS}				1400		
Reverse Transfer Capacitance	C_{RSS}				73		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 50 A			41		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 50 A			89		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 50 A			8.6		
Gate−to−Source Charge	Q_{GS}				15		
Gate−to−Drain Charge	Q_{GD}				10		
Plateau Voltage	V_{GP}				2.8		V
Output Charge	Q_{OSS}	V_{GS} = 0 V, V_{DS} = 20 V			62		nC
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 50 A, R_G = 2.5 Ω			17		ns
Rise Time	t_r				130		
Turn−Off Delay Time	$t_{d(OFF)}$				40		
Fall Time	t_f				14		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.79	1.2	V
			T_J = 125°C		0.64		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 50 A			59		ns
Charge Time	t_a				31		
Discharge Time	t_b				28		
Reverse Recovery Charge	Q_{RR}				80		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
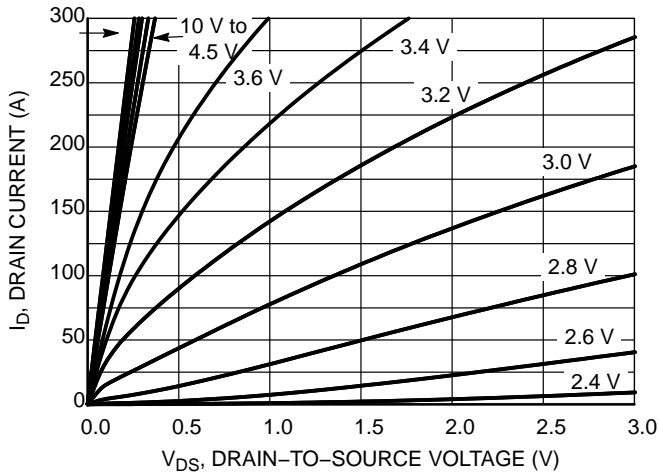
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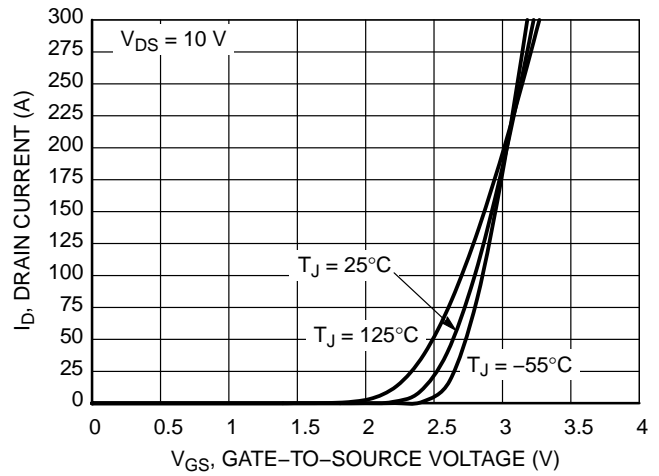## TYPICAL CHARACTERISTICS

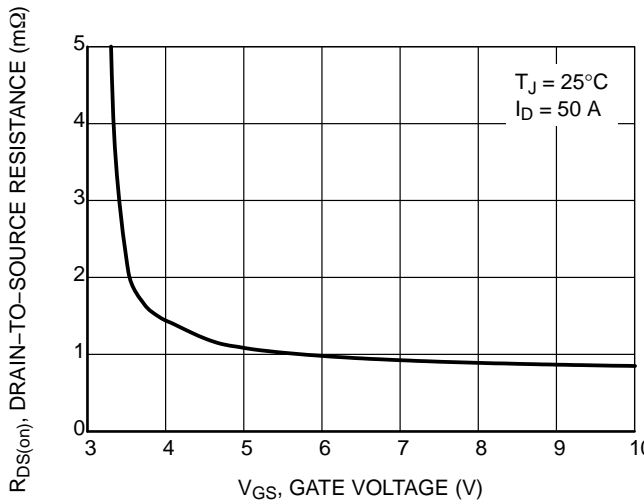Figure 1. On−Region Characteristics

Figure 2. Transfer Characteristics
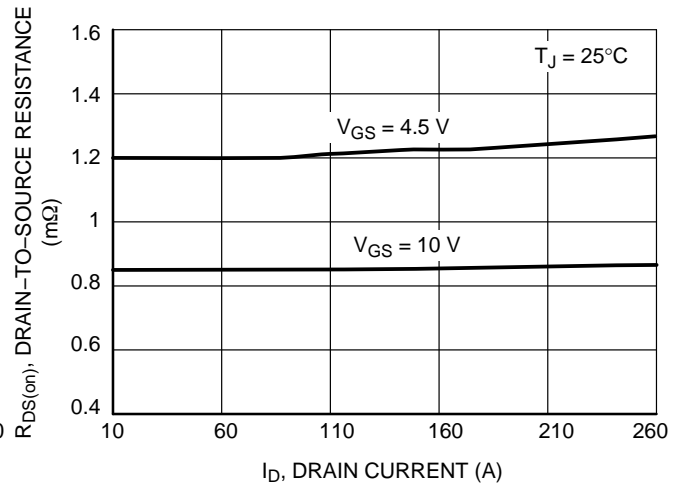
Figure 3. On−Resistance vs. Gate−to−Source
Voltage
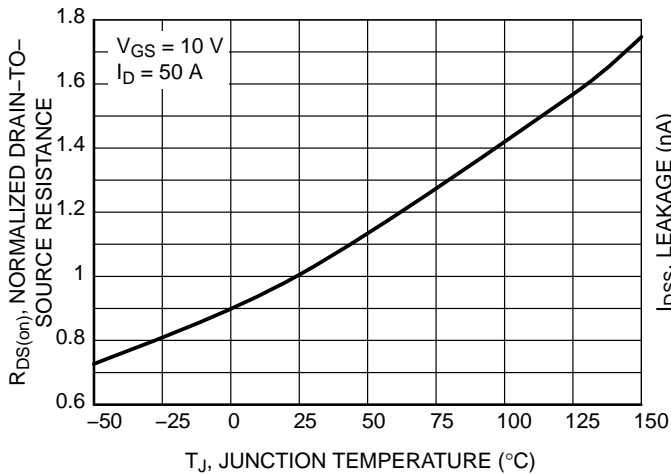
Figure 4. On−Resistance vs. Drain Current and
Gate Voltage

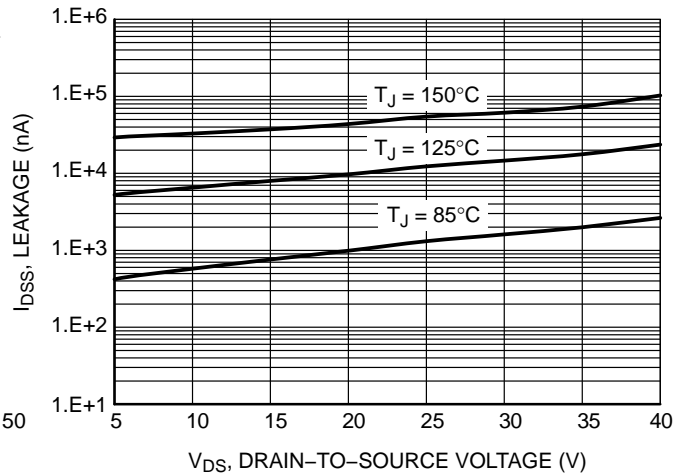Figure 5. On−Resistance Variation with
Temperature

Figure 6. Drain−to−Source Leakage Current
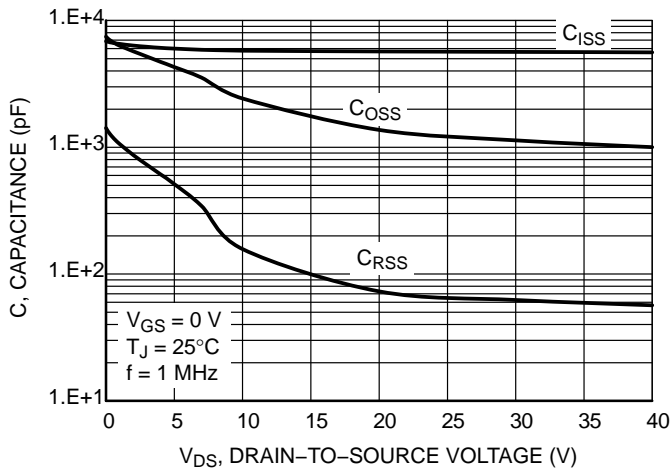vs. Voltage

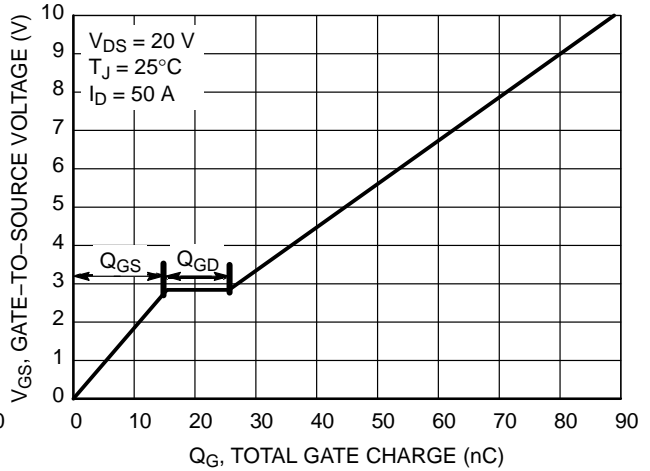## TYPICAL CHARACTERISTICS

Figure 7. Capacitance Variation
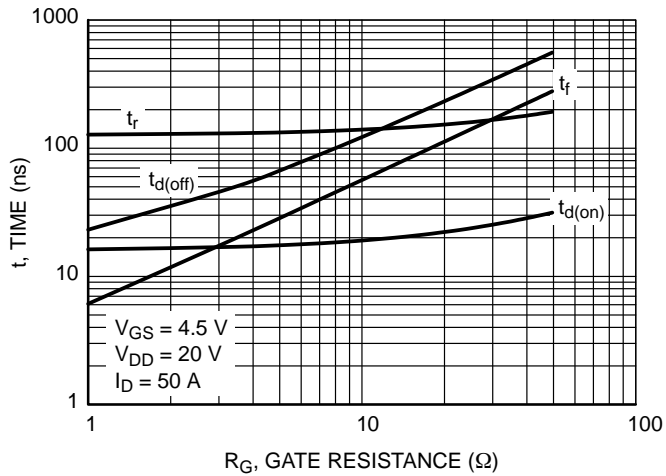

Figure 8. Gate–to–Source vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
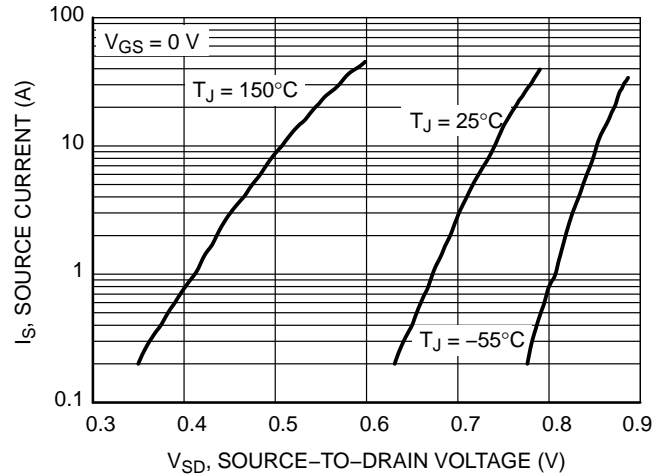
Figure 10. Diode Forward Voltage vs. Current
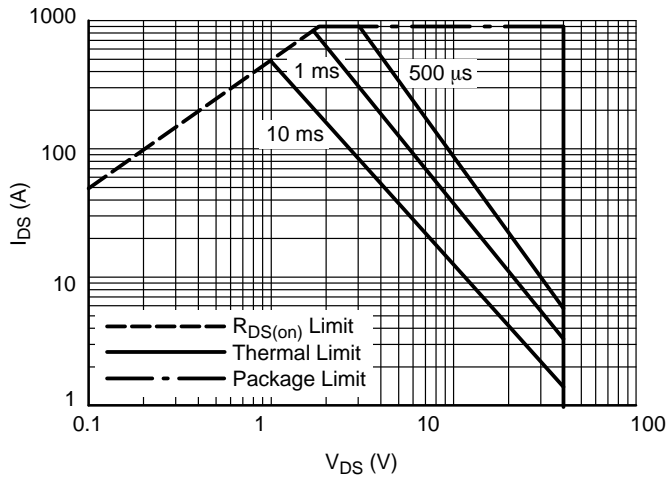
Figure 11. Safe Operating Area
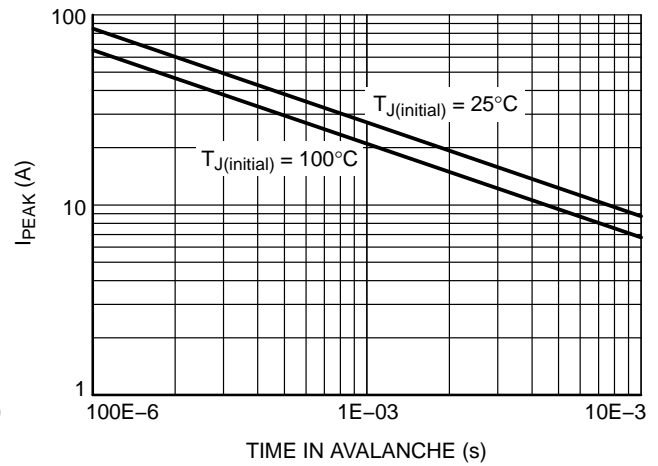
Figure 12. I_{PEAK} vs. Time in Avalanche

NTMFS5H409NL

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS5H409NLT1G	5H409L	DFN5 (Pb–Free)	1500 / Tape & Reel
NTMFS5H409NLT3G	5H409L	DFN5 (Pb–Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO–8FL)
CASE 488AA
ISSUE M

TOP VIEW

SIDE VIEW

DETAIL A

BOTTOM VIEW

PIN 5 (EXPOSED PAD)

DETAIL A

SEATING PLANE
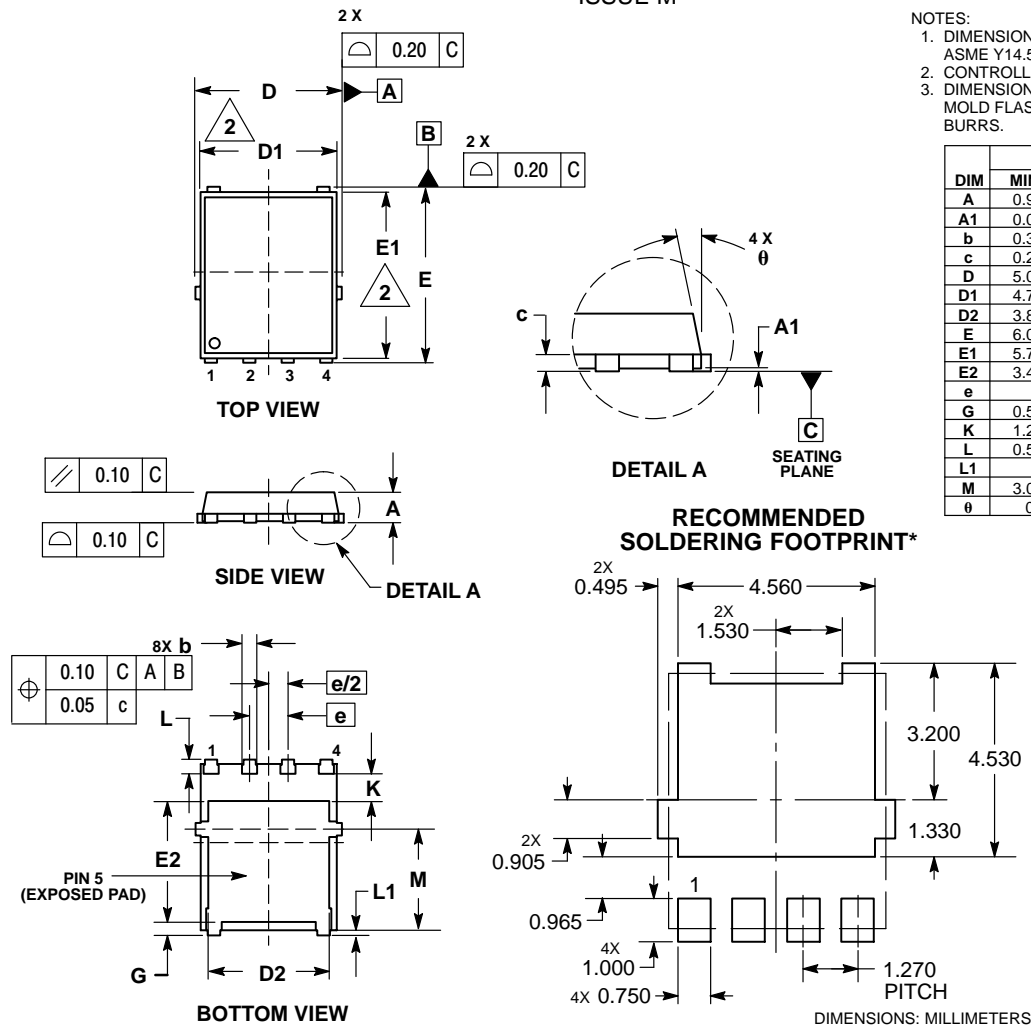
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTMFS5H409NL/D

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